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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,648	02/22/2002	Tze-Chiang Chen	FIS920010243US1	6800

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EXAMINER	
DEO, DUY VU NGUYEN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/082,648	CHEN ET AL.
	Examiner	Art Unit
	DuyVu n Deo	1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-10* is/are rejected.

7)☒ Claim(s) *4 and 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/22/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claim 1, 3, 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Aton (US 6,486,525).

Aton describes a deep trench isolation framed around the transistor of a MOS DRAM (claimed memory storage) (col. 1, line 35-37; col. 2, line 9-12; col. 4, line 1-13). The memory can be an embedded memory in a logic device (col. 5, line 40-43) (this would form a trench between the memory storage region and the logic circuit region). The deep trench is filled with

non-conductive material (or insulating material). Even though Aton is silent about the deep trench isolation prevents the propagation of crystal defects generated in the logic circuit region from propagating into the memory storage; however, he teaches a same structure as that of the claimed invention, and furthermore he teaches that it acts as an insulative barrier against unwanted charges in either the trench or outside the frame (col. 4, line 26-35). Therefore, it would also provide claimed benefit of preventing the propagation of crystal defects generated in the logic circuit region from propagating into the memory storage.

Referring to claim 3, figure 6 show at least 2 trenches formed surrounding the memory storage region.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aton as applied to claim 1 above, and further in view of admitted prior art.

Referring to claims 6 and 7, admitted prior art (pages 1, 3 and 4 of the specification) further describes other structures of eDRAM (or embedded memory in a logic device described by Aton above) including deep trench storage capacitors, CMOS devices and a high dose of impurity layer implanted within a substrate of the logic circuit region to inhibit parasitic bipolar transistor action between the CMOS devices. Therefore, it would have been obvious for one

skilled in the art at the time of the invention to form an embedded memory in a logic device in light of admitted prior art because it further describes other structures of eDRAM with a reasonable expectation of success.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aton as applied to claim 1 above, and further in view of admitted prior art and Wu (US 6,137,152).

Unlike claimed invention, Aton doesn't describe the deep trench is formed beneath a shallow trench isolation. However, he describes eDRAM which, as known to one skilled in the art and described in pages 1 and 2 of the specification, includes CMOS area and having latch-up problem. Wu describes a deep trench formed beneath a shallow trench for isolation CMOS and bipolar devices (or logic circuit region) (ab.; col. 3, line 20-25). It would have been obvious for one skilled in the art to modify Aton in light of Wu because Wu teaches that this structure of isolation would improve the above latch-up problem and packing density of the CMOS/bipolar circuits (col. 3, line 25-30).

6. Claim 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art and Wu (US 6,137,152).

Admitted prior art, pages 1, 2, and 4, describes a conventional eDRAM having logic circuit region 14 and embedded memory storage region 12, a shallow trench isolation 28 for insulating the devices within the memory storage region from devices within the logic circuit region. Unlike claimed invention, conventional described above doesn't teach a deep trench formed underneath the shallow trench isolation. Wu describes a deep trench formed beneath a shallow trench for isolation CMOS and bipolar devices (or logic circuit region) (ab.; col. 3, line 20-25). It would have been obvious for one skilled in the art to modify admitted prior art in light

of Wu because Wu teaches that this structure of isolation would improve the above latch-up problem and packing density of the CMOS/bipolar circuits (col. 3, line 25-30).

7. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art and Wu as applied to claim 8 above, and further in view of Aton (US 6,486,525).

Unlike claimed invention, admitted prior art doesn't describe the trench isolation 28 surrounding the memory storage region 12. Aton teaches forming deep trench around the DRAM or memory region (col. 1,line 35-37; col. 2, line 10-13). It would have been obvious for one skilled in the art at the time of the invention to form the trench isolation around the memory region because Aton teaches that it would act as an insulative barrier against unwanted charges in either the trench or outside the frame (col. 4, line 27-35).

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for having a memory storage region 12 next to the logic circuit region, does not reasonably provide enablement for a memory storage region embedded within the logic circuit region. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. Figure 2 shows the memory region 12 is not formed within the logic circuit region 14. At this time, it is understood as formed next to the logic circuit region.

Allowable Subject Matter

10. Claims 4, 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4 and 11-13 are allowable because applied prior art doesn't describe or suggest the deep trench isolations comprises an inner and outer perimeter, wherein individual deep trench isolations included in the outer perimeter are disposed adjacent to gaps in between individual deep trench isolations included in the inner perimeter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 571-272-1462. The examiner can normally be reached on 6:00-3:30; with alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DVD
5/4/04